IN THE DRAWINGS:

The attached Replacement Sheets of drawings includes changes to Figs. 1 and 5. The Replacement Sheet for Fig. 1 includes newly added labels identifying surface channel and buried channel MOS transistors; and the Replacement Sheet for Fig. 5 includes the newly added label identifying the figure as "PRIOR ART." No other changes have been made to Figs. 1 and 5.

Attachments: Replacement Sheets (2 sheets)

## REMARKS

The present application has been reviewed in light of the Office Action dated November 17, 2008. Claims 11-16 are presented for examination, of which Claims 11 and 12 are in independent form. New Claims 17 and 18 have been added to provide Applicants with a more complete scope of protection. Claims 11-16 have been amended to define aspects of Applicant's invention more clearly. Favorable reconsideration is requested.

The Office Action states that the drawings are objected to, because of the following informalities:

(a) Vr1, Vsig1-Vr1, VFDsig1, Qsig, etc., are mentioned in paragraphs [0035]-[0040] but are not shown in the drawings;

(b) buried channel and surface channel MOS transistors are not labeled in the drawings; and

(c) Fig. 5 is not labeled as "Prior Art."

In response to items (b) and (c) of the objection to the drawings, the attached Replacement Sheets of drawings includes changes to Figs. 1 and 5. The Replacement Sheet for Fig. 1 includes newly added labels identifying surface channel type and buried channel type MOS transistors; and the Replacement Sheet for Fig. 5 includes the newly added label identifying the figure as "PRIOR ART." No other changes have been made to Figs. 1 and 5. Applicant submits that the amendments to the drawings add no new matter to the original disclosure, and support for the amendments may be found, for example, in paragraphs [0031] and [0032] of U.S. Patent Application Publication No. 2008/0224146 corresponding to the present application. Approval

of the amended drawings and withdrawal of items (b) and (c) of the objection to the drawings are respectfully requested.

In response to item (a) of the objection to the drawings, Applicant submits that Vr1, Vsig1-Vr1, VFDsig1, and Qsig are signals, which are not structural features that can be represented in drawings easily. It is respectfully submitted that persons of ordinary skill in the art would understand what these quantities represent without the use of an illustration. Accordingly, withdrawal of item (a) of the objection to the drawings is respectfully requested.

The Office Action indicates, at item 12 on page 1, that no certified copy of the foreign priority document has been received for the present application. Applicant submits, however, that the present application is a U.S. national-stage entry of International Application No. PCT/JP2005/006226, and the certified copy of the foreign priority document was provided to the International Bureau as part of the PCT Request of the International Application. Accordingly, Applicant respectfully requests acknowledgment of the receipt of the certified copy in International Application No. PCT/JP2005/006226.

The Office Action states that Claim 11 is rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Publication No. 2004/0263657 (Sakamoto et al.); that Claims 12, 15, and 16 are rejected under § 103(a) as being unpatentable over U.S. Patent No. 6,100,551 (Lee et al.) in view of Sakamoto et al.; and that Claims 13 and 14 are is rejected under § 103(a) as being unpatentable over Lee et al. in view of Sakamoto et al., and further in view of U.S. Patent No. 5,880,494 (Watanabe). For at least the reasons presented below, Applicant submits that independent Claims 11 and 12, together with the claims dependent therefrom, are patentably distinct from the cited references.

Claim 11 is directed to a method of manufacturing a semiconductor apparatus provided with both a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor. According to the method, a first conductive type impurity region is formed in respective channel positions of the buried channel type MOS transistor and the surface channel type MOS transistor in a same step, such that a lowest potential region is arranged in an area that is at a predetermined depth from a surface of an image pickup device of the semiconductor apparatus.

Sakamoto et al. relates to an image pickup device with a horizontal transfer path. It is alleged in the Office Action that Sakamoto et al. teaches a buried channel type first conductive type MOS transistor at reference numeral 68 of Figs. 5A and 5B, and teaches a surface channel type first conductive type MOS transistor at reference numeral 62 of Figs. 5A and 5B. Applicant respectfully disagrees with this characterization of Sakamoto et al.

It is respectfully submitted that Sakamoto et al. is completely silent regarding a buried channel type MOS transistor, and that reference numerals 62 and 68 pointed out in the Office Action do not in fact represent a surface channel type MOS transistor and a buried channel type MOS transistor, respectively. More specifically, as understood by Applicant, Sakamoto et al. teaches a charge accumulation electrode 62 and a reset gate electrode 67, and also teaches that under the charge accumulation electrode 62 and the reset gate electrode 67 the *same* horizontal charge transfer channel is formed. Also, the regions under the electrodes 62 and 67 have the *same* impurity profile. Because the same channel is formed under these electrodes 62 and 67, these electrodes cannot represent a surface channel type MOS transistor and a buried channel type MOS transistor, respectively. Moreover, Sakamoto et al. neither discloses nor suggests making

these regions have different impurity profiles, such that "a lowest potential region is arranged in an area that is at a predetermined depth from a surface" of the image pickup device.

In summary, nothing has been found in Sakamoto et al. that is believed to teach or suggest a method of manufacturing a semiconductor apparatus provided with both a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor, in which the method includes "forming a first conductive type impurity region in respective channel positions of said buried channel type MOS transistor and said surface channel type MOS transistor in a same step, such that a lowest potential region is arranged in an area that is at a predetermined depth from a surface of an image pickup device of said semiconductor apparatus," as recited in Claim 11. Accordingly, Applicant submits that Claim 11 is not anticipated by Sakamoto et al. and therefore respectfully requests withdrawal of the rejection under 35 U.S.C. § 102(b).

Applicant notes that Sakamoto et al. is effective as prior art as of its U.S. filing date: May 19, 2004. The present application has a priority date of March 30, 2004, based on Japanese Application No. 2004-099346. Thus, the foreign priority date of the present application is before the date that Sakamoto et al. is effective as prior art. Applicant intends to submit a sworn English translation of the Japanese priority application shortly, in order to remove Sakamoto et al. as a reference that may be cited against the claims of the present application.

In regard to Claim 12, this claim has a forming step that is similar to the forming step of Claim 11.

Lee et al. relates to a pixel sensor integrated with a pinned photodiode. As understood by Applicant, Lee et al. discloses that a buried channel photocapacitor can be used in

place of the pinned photodiode (see, for example, the abstract), but does not disclose or suggest a method for manufacturing a device structure that includes both buried channel type and surface channel type MOS transistors, in which a first conductive type impurity region is formed in respective channel positions of the buried channel type MOS transistor and the surface channel type MOS transistor, such that a lowest potential region is arranged in an area that is at a predetermined depth from a surface of the device. Thus, it is respectfully submitted that Lee et al. suffers from the same deficiencies as Sakamoto et al.

In summary, Applicant submits that a combination of Lee et al. and Sakamoto et al., assuming such combination would even be permissible, would fail to teach or suggest a method of manufacturing a solid state image pickup device with a buried channel type first conductive type MOS transistor and a surface channel type first conductive type MOS transistor, in which the method includes "forming a first conductive type impurity region in respective channel positions of said buried channel type MOS transistor and said surface channel type MOS transistor, such that a lowest potential region is arranged in an area that is at a predetermined depth from a surface of the image pickup device," as recited in Claim 12. Accordingly, Applicant submits that Claim 12 is patentable over any permissible combination of Lee et al. and Sakamoto et al., and respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a).

Independent Claim 18 includes a forming step similar to those of Claims 11 and 12, and is believed to be patentable for at least the reasons discussed above. Also, the other claims in the present application depend from Claim 12 and therefore are submitted to be patentable for at least the same reasons. However, because each dependent claim also is deemed

to define an additional aspect of the invention, individual consideration or reconsideration, as the case may be, of the patentability of each claim on its own merits is respectfully requested.

Support for the changes to Claims 11 and 12 may be found, for example, in paragraph [0042] of U.S. Patent Application Publication No. 2008/0224146 corresponding to the present application. Support for the changes to Claim 13 may be found, for example, in paragraph [0045] of U.S. Patent Application Publication No. 2008/0224146 corresponding to the present application. Support for new Claim 17 may be found, for example, in the third embodiment disclosed in U.S. Patent Application Publication No. 2008/0224146 corresponding to the present application. Support for new Claim 18 may be found, at least in part, in paragraphs [0042] and [0045] of U.S. Patent Application Publication No. 2008/0224146 corresponding to the present application.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and an early passage to issue of the present application.

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Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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